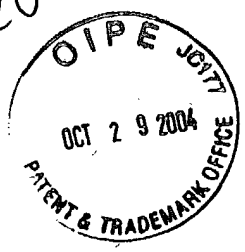
120



AF/2673

Docket No.: SON-1582/SUG
(80063-0004)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu Ino et al.

Confirmation No.: 8128

Application No.: 09/424,544

Art Unit: 2673

Filed: November 24, 1999

Examiner: J. J. Piziali

For: LIQUID CRYSTAL DISPLAY

RESPONSE TO NOTICE OF NON-COMPLIANCE

MS Appeal Brief- Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Notice of Non-compliance mailed on October 21, 2004. The Notice of Non-Compliance contends that the Appeal Brief filed on July 21, 2004 does not contain a correct copy of the appeal claims as an appendix thereto.

In response to the Notice of Non-Compliance, an Appeal Brief is provided.

Dated: October 29, 2004

Respectfully submitted,

By_____
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Docket No.: SON-1582/SUG
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Filed: November 24, 1999

Examiner: J. J. Piziali

For: LIQUID CRYSTAL DISPLAY

TRANSMITTAL OF APPEAL BRIEF

MS Appeal Brief- Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Three copies of an Appellant's Brief on Appeal for the above-referenced application are being filed herewith. An Appeal Brief and fee was filed on April 2, 2004. Thus, it is believed that **no fees are due**. M.P.E.P. §1208.02.

Consideration of the Appeal Brief is respectfully requested.

Dated: October 29, 2004

Respectfully submitted,

By_____
Ronald P. Kananen
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu Ino et al.

Application No.: 09/424,544 Confirmation No.: 8128

Filed: November 24, 1999 Art Unit: 2673

For: LIQUID CRYSTAL DISPLAY Examiner: J. J. Piziali

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated November 4, 2003. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately.

This brief is in furtherance of the Final Office Action on November 4, 2003.

A Notice of Appeal was filed in this case on February 4, 2004.

This brief is transmitted in triplicate.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 010555, frame 0866.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-20 were originally filed in this application.

By the amendment filed on February 27, 2002, claims 9 and 16 have been amended, and claims 21-39 added.

By the amendment filed on September 16, 2002, claims 3 and 38 have been amended, and claims 40-42 added.

By the amendment filed on February 26, 2003, claims 1-2, 10, 12-13, 21-22, 30, 32-36, and 38-42 have been canceled, claims 3, 11, 13, 15, 17-20, 25-27 and 37 have been amended, and claims 43-48 added.

By the amendment filed on August 20, 2003, claim 3 has been amended.

The Amendment After Final Rejection Under 37 C.F.R. § 1.116 filed on February 4, 2004 proposed the cancellation of claims 3, 5, 7, 11, 13-20 and 23-42, proposed an amendment to claims 6 and 25, and proposed the addition of claims 49-66. However, the Advisory Action of February 25, 2004 indicated that the Amendment After Final Rejection Under 37 C.F.R. § 1.116 of February 4, 2004 had not been entered.

The Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 filed on March 8, 2004 proposed the cancellation of claims 3, 5, 7, 11, 13-20 and 23-42, proposed an amendment to claims 6 and 25, and proposed the addition of claims 49-60. The Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 filed on March 8, 2004 proposed the addition of claims 61-66.

However, the Advisory Action of July 21, 2004 indicated that the Second and Third Amendments After Final Rejection Under 37 C.F.R. § 1.116 had not been entered because both Amendments had been submitted using only one Amendment Transmittal form and that each of the Second and Third Amendments require its own individual Amendment Transmittal form. The Advisory Action indicates that if resubmitted along with its own individual Amendment Transmittal form, the Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 would be considered for entry whereas the Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 would not.

The Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 has been resubmitted on July 22, 2004 as the Fourth Amendment After Final Rejection Under 37 C.F.R. § 1.116 proposes the cancellation of claims 3, 5, 7, 11, 13-20 and 23-42, proposed an amendment to claims 6 and 25, and proposed the addition of claims 49-60.

The Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 resubmitted on July 22, 2004 as the Fifth Amendment After Final Rejection Under 37 C.F.R. § 1.116 proposes the addition of claims 61-66.

Although the Second and Third Amendments After Final Rejection Under 37 C.F.R. § 1.116 have been resubmitted each with their own individual Amendment Transmittal forms in the manner requested by the Advisory Action of July 21, 2004 as the Fourth and Fifth Amendments

After Final Rejection Under 37 C.F.R. § 1.116, the Advisory Action of October 21, 2004 now indicates that the Fourth and Fifth Amendment After Final Rejection Under 37 C.F.R. § 1.116 would not be entered.

Accordingly, appellant hereby appeals the final rejection of claims 3, 5-7, 11, 13-20, 23-29, 31, 37, and 43-48 which are presented in the Claims Appendix.

The status of the claims is as follows:

Claims 1-2 (canceled)

Claim 3 (rejected)

Claim 4 (canceled)

Claims 5-7 (rejected)

Claims 8-10 (canceled)

Claim 11 (rejected)

Claim 12 (canceled)

Claims 13-20 (rejected)

Claims 21-22 (canceled)

Claims 23-29 (rejected)

Claim 30 (canceled)

Claim 31 (rejected)

Claims 32-36 (canceled)

Claim 37 (rejected)

Claims 38-42 (canceled)

Claims 43-48 (rejected)

IV. STATUS OF AMENDMENTS

Subsequent to the final rejection of November 4, 2003, an Amendment After Final Action (37 CFR Section 1.116) has been filed on February 4, 2004.

The Advisory Action of February 25, 2004 indicated that the Amendment After Final Rejection Under 37 C.F.R. § 1.116 of February 4, 2004 had not been entered.

A Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 and a Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 have been filed on March 8, 2004.

The Advisory Action of July 21, 2004 indicated that the Second and Third Amendments After Final Rejection Under 37 C.F.R. § 1.116 had not been entered.

The Fourth and Fifth Amendments After Final Rejection Under 37 C.F.R. § 1.116 have been filed have been filed on July 22, 2004

The Advisory Action of October 21, 2004 indicated that the Fourth and Fifth Amendments After Final Rejection Under 37 C.F.R. § 1.116 had not been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a liquid crystal display (LCD) and, more particularly, to a matrix type liquid crystal display in which a driver circuit to apply a signal potential to each pixel is provided as an external circuit of a liquid crystal display panel.

At least figures 3 and 6 depict a display portion 10 (figure 6) in which a plurality of pixels 20 are two-dimensionally arranged at intersecting points of gate lines 11 as many as a plurality of rows and signal lines 12 as many as a plurality of columns which are wired in a matrix shape (figure 3). A plurality of driver circuits 14 for apply a signal potential to each pixel 20 in the display portion 10 through the signal lines 12 of the plurality of columns.

At least figures 7 and 8 depict time-divisional switches 46 for time-divisionally sending a signal potential that is outputted from each of the plurality of driver circuits 44 to the signal lines 42 of the plurality of columns, wherein a time-dividing number of the time-divisional switches is equal to 3.

As further described within the specification as originally filed, the number of output terminals of each of the plurality of driver circuits is set to a measure of the total number of signal lines of the plurality of columns (page 16, lines 14-18). The number of output terminals of each of the plurality of driver circuits 14 is set to a same number (figure 6). When a size of a frame portion adjacent to the display portion 10 is specified, the number (n) of output terminals of each of the plurality of driver circuits 14 is determined on the basis of the specified frame size by the number of lines which can be wired into a wiring region of the frame portion. When the total number of signal lines 12 of the plurality of columns that is decided by a display system is set to N, the number of driver circuits 14 is set to N/n, wherein the total number of signal lines 12 is different than the number (n) of output terminals (page 15, line 14 to page 16, line 24).

The plurality of driver circuits 14 include driver ICs arranged in an outside of a transparent insulating substrate on which the display portion 10 is formed.

At least figures 2, 3 and 5 depict a display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20. A pixel 20 is located at an intersection of a gate line 11 and a signal line 12 (figure 3). A plurality of driver circuits 14 include at least one general driver circuit 14-1 to 14-25 and one remainder driver circuit 14-26. Each general driver circuit 14-1 to 14-25 has a plurality of general driver circuit output terminals, wherein a general driver circuit output terminal provides a signal potential to one of the plurality of signal lines 12 (figure 2). The remainder driver circuit 14-26 has a plurality of remainder driver circuit output terminals, wherein a remainder driver circuit output terminal provides another signal potential to another of the plurality of signal lines 12 (figure 5).

The quantity of the remainder driver circuit output terminals is defined as (S – (OP * (DC-1))), "S" being the quantity of the plurality of signal lines 12, "OP" being the quantity of the general driver circuit output terminals, and "DC" being the quantity of the plurality of driver circuits, wherein the quantity of the general driver circuit output terminals is different than the quantity of the remainder driver circuit output terminals (page 13, lines 10-26).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 were rejected under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent 4,825,203 issued to Takeda et al. (Takeda).

This issue will be discussed hereinbelow.

VII. ARGUMENT

In the Office Action of November 4, 2003:

The Examiner rejected claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 under 35 U.S.C. 102 as allegedly being anticipated by Takeda.

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below.

Claim Groups:

Claims 3, 5, 7, 11, 13-20 and 23-24 stand or fall together.

Claim 6 stands or falls separately.

Claim 25-29, 37, 43-47 stand or fall together.

Claim 31 stands or falls separately.

Claim 48 stands or falls separately.

The Examiner erred in rejecting claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 under 35 U.S.C. 102 as allegedly being anticipated by Takeda.

This rejection is respectfully traversed for at least the following reasons.

Claim 6

Claim 6 is dependent upon claim 3. Claim 3 includes

a display portion 10 (specification at figure 6) in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines 41 as many as a plurality of rows and signal lines 42 as many as a plurality of columns which are wired in a matrix shape (specification at figure 7, page 18, lines 20-27);

a plurality of driver circuits 44 for applying a signal potential to each pixel in said display portion through the signal lines 42 of said plurality of columns (specification at figure 7, page 19, lines 16-21); and

time-divisional switches 46 for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits 44 to the signal lines 42 of said plurality of columns (specification at figures 7-9, page 20, line 25 to page 23, line 21),

characterized in that a time-dividing number of said time-divisional switches 46 is equal to 3 (specification at page 36, line 27),

the number of output terminals 45 of each of said plurality of driver circuits 44 is set to a measure of the total number of signal lines 42 of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number (specification at figure 8, page 21, lines 14-24),

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion (specification at page 44, line 17 to page 45, line 4),

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the number of said driver circuits is set to N/n, said total number of signal lines being different than said number (n) of output terminals (specification at page 44, lines 23-26).

Claim is dependent upon claim 3. Within claim 6, said plurality of driver circuits 44 are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion 10 is formed (specification at figure 6).

Rejected claim 6, which has been amended to place that claim into independent form, is characterized in that the plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which the display portion is formed.

However, a review of Takeda reveals that a "substrate" is not found therein. In addition, Takeda is silent as to the substrate being a "transparent insulating substrate".

Moreover, U.S. Patent No. 6,788,380 to Melnik et al., which is provided as an attachment to this Appeal Brief within the Evidence Appendix, teaches the presence of silicon substrate 110 (Melnik at figure 1, column 1, lines 29-30) and silicon substrate 210 (Melnik at figure 2, column 2, lines 58-59). As shown in Melnik by the presence of silicon substrates 110 and 210, **a transparent insulating substrate is not inherent**.

Because a "substrate" or a "transparent insulating substrate" is not found within Takeda, all features within claim 6 are not found within Takeda, and because a transparent insulating substrate is not inherent as shown by Melnik et al., the final rejection of at least claim 6 is improper and premature as a result.

In addition, rejected claim 6 provide that when a size of a frame portion adjacent to the display portion is specified, the number (n) of output terminals of each of the plurality of driver circuits is determined on the basis of the specified frame size by the number of lines which can be wired into a wiring region of the frame portion, and when the total number of signal lines of the plurality of columns that is decided by a display system is set to N, the number of the driver circuits is set to N/n, the total number of signal lines being different than the number (n) of output terminals.

The Final Office Action cites elements q_1-q_N of Takeda as the plurality of driver circuits. While figure 1(A) of Takeda arguably depicts elements q_1-q_N at the output of shift register 31, the

description found within Takeda fails to provide, with particularity, a written definition for elements q_1-q_N.

Instead, Takeda arguably teaches that "the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line" (figures 1(A),(B), column 4, lines 29-31), that "the signals required for sequential display are input to the gate circuit (37) from the shift register" (column 4, lines 59-61), and that "a shift register (31) that outputs signals to each column electrode line corresponding to the display pattern" (figure 5(A), column 6, lines 12-14). As shown above, Takeda arguably teaches elements q_1-q_N as "signals" while failing to disclose, teach or suggest elements q_1-q_N as "a plurality of driver circuits".

Moreover, calculations provided within the Final Office Action arguably teach the total number of signal lines in Takeda as being ***the same as*** the number (n) of output terminals of each of the plurality of driver circuits. However, the claimed invention provides that the total number of signal lines ***is different*** than the number (n) of output terminals of each of the plurality of driver circuits.

Claims 3, 5, 7, 11, 13-20 and 23-24

While not conceding the propriety of these rejections, and in order to further the prosecution of the application, claims 3, 5, 7, 11, 13-20 and 23-24 attempts have been made within the above-noted Amendments After Final Rejection Under 37 C.F.R. § 1.116 to cancel these claims without prejudice or disclaimer of their underlying subject matter, rendering the rejection moot as to these claims.

Claims 25-29, 37, 43-47

Claim 25 includes the features of:

a display portion 10 (specification at figure 5), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3); and

a plurality of driver circuits 14, 44 (specification at page 19, lines 5-6), said plurality of driver circuits 14, 44 including at least one general driver circuit and one remainder driver circuit (specification at figure 5),

each said at least one general driver circuit 14, 44 having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals 14, 44 providing a signal potential to one of said plurality of signal lines (specification at page 19, lines 5-6),

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (specification at figure 5),

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21), "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13), "OP" being the quantity of general driver circuit output terminals , and "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26),

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals (specification at figure 5).

Claim 25 and the claims dependent thereon comprise a plurality of driver circuits including at least one general driver circuit wherein a general driver circuit output terminal provides a signal potential to one of the plurality of signal lines. The plurality of driver circuits further includes one remainder driver circuit wherein a remainder driver circuit output terminal provides another signal potential to another of the plurality of signal lines.

The Final Office Action contends that Takeda depicts row electrodes 11-a as a plurality of gate lines 11-a and column electrodes 11-b as a plurality of signal lines 11-b. Thus, the Final Office Action identifies the row electrodes 11-a as the plurality of gate lines 11-a, and not as the plurality of signal lines.

But while figure 1(A) of Takeda arguably depicts plurality of driver circuits having a column electrode drive circuit 13 (column 4, line 23) providing signals to column electrodes 11-b (column 3, lines 4-6), and figure 3(A) of Takeda arguably depicts a row electrode drive circuit 121,122 (column 4, lines 11-12) providing signals to row electrodes 11-a (column 3, lines 1-2), Takeda fails to disclose, teach or suggest both the column electrode drive circuit 13 and the row electrode drive circuit 121,122 providing signal potentials to column electrodes 11-b.

Thus, Takeda fails to disclose, teach or suggest column electrode drive circuit 13 and the row electrode drive circuit 121,122 as the plurality of driver circuits found within claim 25 and the claims dependent thereon since the claimed plurality of driver circuits provide a signal potential to the plurality of signal lines whereas the row electrode drive circuit 121,122 of Takeda provides signal potentials to the row electrodes 11-a and not to the column electrodes 11-b.

The Final Office Action cites elements q_1-q_N of Takeda as the plurality of driver circuits. While figure 1(A) of Takeda arguably depicts elements q_1-q_N at the output of shift register 31, the description found within Takeda fails to provide, with particularity, a written definition for elements q_1-q_N. Instead, Takeda arguably teaches that "the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line" (figures 1(A),(B), column 4, lines 29-31), that "the signals required for sequential

display are input to the gate circuit (37) from the shift register" (column 4, lines 59-61), and that "a shift register (31) that outputs signals to each column electrode line corresponding to the display pattern" (figure 5(A), column 6, lines 12-14). As shown above, Takeda arguably teaches elements q_1-q_N as "signals" while failing to disclose, teach or suggest elements q_1-q_N as "a plurality of driver circuits".

Also note that figure 1(A) of Takeda depicts buffer 36 as having only a single output Q_N, and not two (2) outputs as contended within the Office Action, and that a single signal q_N shown within figure 1(A) of Takeda corresponds only to a single output Q_N.

Moreover, claim 25 and the claims dependent thereon provide that the quantity of general driver circuit output terminals are different than the quantity of remainder driver circuit output terminals. But as shown within figure 1(A) there is the same quantity of outputs from each of the buffers 36, there is the same quantity of outputs from each of the analog switches 32, 34, and there is the same quantity of outputs from each of the gate circuits 37.

The Final Office Action further contends that each general driver circuit has a plurality of general driver circuit output terminals 36. But since each of the signals q_1-q_N of Takeda are uniquely associated with a buffer 36, this contention is inconsistent at least with the other contention regarding claim 25 made within the Final Office Action that elements q_1-q_N of Takeda are the plurality of driver circuits.

The Final Office Action asserts without provided any evidentiary support that there are two (2) remainder driver circuit output terminals, five (5) plurality of signal lines, three (3) general driver circuit output terminals, and two (2) plurality of driver circuits.

In response, this unsupported assertion amounts to nothing more than conclusions that are personal in nature because the cited prior art does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. In this regard, the teachings, suggestions or incentives supporting the rejection must be clear and particular.

Claim 31

The rejection of this claim is traverse at least for the reasons provided hereinabove with respect to claim 25 and for the following reasons.

Claim 31 includes a surplus connecting region that does not contribute to said display portion does not occur on the said display (specification page 16, lines 22-24).

However, Takeda fails to disclose, teach or suggest a surplus connecting region that does not contribute to the display portion which does not occur on the display. The Final Office Action cites elements 12, 13 and 15 of Takeda for this teaching. But in this regard, element 12 of Takeda contributes to the display portion as the row electrode drive circuit (Takeda at column 3, line 1), element 13 of Takeda contributes to the display portion as the column electrode drive circuit (Takeda at column 3, line 4), and element 15 of Takeda contributes to the display portion as the control circuit (Takeda at column 3, line 8).

Claim 48

The rejection of this claim is traverse at least for the reasons provided hereinabove with respect to claim 25 and for the following reasons.

Within claim 48, the plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (specification at figure 5).

However, a review of Takeda reveals that a "substrate" is not found therein. In addition, Takeda is silent as to the substrate being a "transparent insulating substrate".

Moreover, U.S. Patent No. 6,788,380 to Melnik et al., which is provided as an attachment to this Appeal Brief within the Evidence Appendix, teaches the presence of silicon substrate 110 (Melnik at figure 1, column 1, lines 29-30) and silicon substrate 210 (Melnik at figure 2, column 2, lines 58-59). As shown in Melnik by the presence of silicon substrates 110 and 210, **a transparent insulating substrate is not inherent**.

Because a "substrate" or a "transparent insulating substrate" is not found within Takeda, all features within claim 48 are not found within Takeda, and because a transparent insulating substrate is not inherent as shown by Melnik et al., the final rejection of at least claim 48 is improper and premature as a result.

Conclusion

The Office Action fails to show that **each and every element** as set forth in the claim is found, either expressly or inherently described, solely within Takeda, **which is a specific requirement of an anticipation rejection made pursuant to 35 U.S.C. §102.**

Accordingly, Takeda does not anticipate Applicant's invention. The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

A copy of the claims involved in the present appeal is attached hereto as the Claims Appendix.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: October 29, 2004

Respectfully submitted,

By_____

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CLAIMS APPENDIX

1-2 (canceled).

3. (previously presented) A liquid crystal display comprising:

a display portion in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines as many as a plurality of rows and signal lines as many as a plurality of columns which are wired in a matrix shape;

a plurality of driver circuits for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns; and

time-divisional switches for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits to the signal lines of said plurality of columns,

characterized in that a time-dividing number of said time-divisional switches is equal to 3,

the number of output terminals of each of said plurality of driver circuits is set to a measure of the total number of signal lines of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number,

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said

specified frame size by the number of lines which can be wired into a wiring region of said frame portion,

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the number of said driver circuits is set to N/n, said total number of signal lines being different than said number (n) of output terminals.

4. (canceled).

5. (original) A display according to claim 3, characterized in that the number of output terminals of each of said plurality of driver circuits is set to a power of 2.

6. (original) A display according to claim 3, characterized in that said plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion is formed.

7. (original) A display according to claim 3, characterized by comprising:

a memory circuit for temporarily storing data to be written into said plurality of driver circuits; and

a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

8-10. (canceled).

11. (previously presented) A display according to claim 3, characterized in that a leading waveform and a trailing waveform of a signal output waveform of each of said plurality of driver circuits are symmetrical with respect to a time base.

12. (canceled).

13. (previously presented) A display according to claim 3, characterized in that a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period.

14. (original) A display according to claim 13, characterized in that a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches.

15. (previously presented) A display according to claim 3, characterized in that a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal scanning period – the period of time selected by the time-divisional switches x 3) / 3.

16. (previously presented) A display according to claim 15, characterized in that said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period.

17. (previously presented) A display according to claim 3, characterized in that said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) by diving to said time-divisional switches.

18. (previously presented) A display according to claim 3, characterized in that in a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red.

19. (previously presented) A display according to claim 3, characterized in that in a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue.

20. (previously presented) A display according to claim 3, characterized in that time-division of said time-division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel.

21-22. (canceled).

23. (previously presented) A display according to claim 3, characterized in that a surplus connecting region that does not contribute to said display portion does not occur on the said display.

24. (previously presented) A display according to claim 3, characterized in that a driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

25. (previously presented) A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits,

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals.

26. (previously presented) A display according to claim 25, wherein each driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

27. (previously presented) A display according to claim 25, wherein said plurality of pixels is arranged in a two-dimensional matrix shape.

28. (previously presented) A display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line.

29. (previously presented) A display according to claim 25, wherein said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns.

30. (canceled).

31. (previously presented) A display according to claim 25, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

32-36. (canceled).

37. (previously presented) A display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

38-42. (canceled).

43. (previously presented) A display according to claim 37, wherein said plurality of primary colors is a first primary color, a second primary color and a third primary color.

44. (previously presented) A display according to claim 25, wherein said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals.

45. (previously presented) A display according to claim 25, wherein the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines.

46. (previously presented) A display according to claim 25, wherein said plurality of driver circuits include more than one said general driver circuit.

47. (previously presented) A display according to claim 46, wherein each said general driver circuit has an equal number of general driver circuit output terminals.

48. (previously presented) A display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

EVIDENCE APPENDIX

1. U.S. Patent No. 6,788,380 to Melnik et al.

US006788380B2

(12) **United States Patent**
Melnik et al.

(10) **Patent No.: US 6,788,380 B2**
(45) **Date of Patent: Sep. 7, 2004**

(54) **LIQUID CRYSTAL DISPLAY DEVICE HAVING UNIFORM INTEGRATED SPACERS**

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(21) Appl. No.: **10/685,862**

(22) Filed: **Oct. 15, 2003**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**[7] **G02F 1/1339**; G02F 1/1345

(52) **U.S. Cl.** **349/156**; 349/149

(58) **Field of Search** 349/156, 149, 349/152, 44

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,682,858 A * 7/1987 Kanbe et al. 349/156

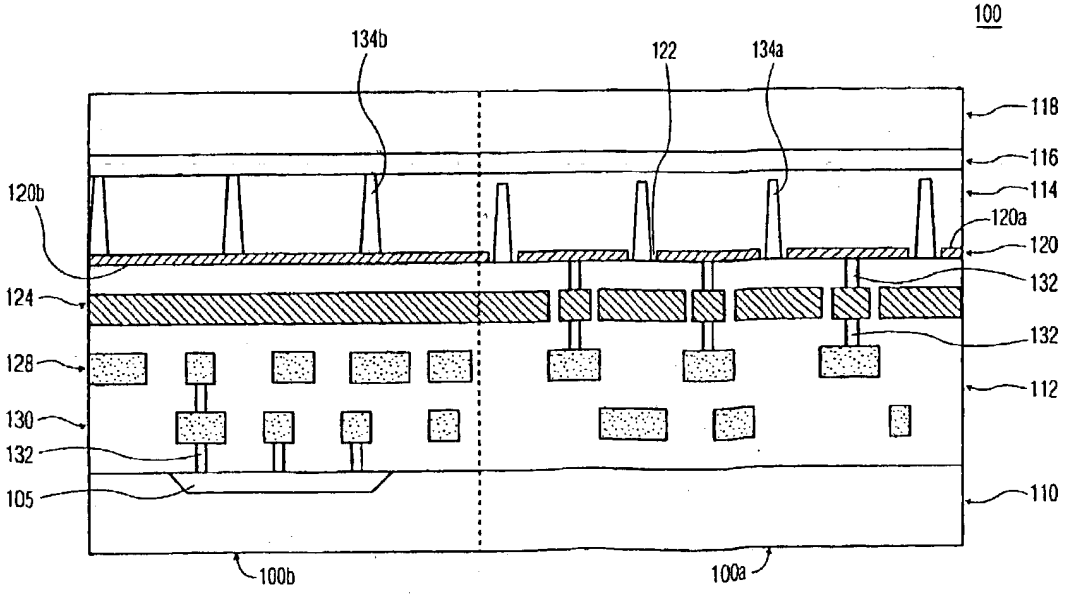
* cited by examiner

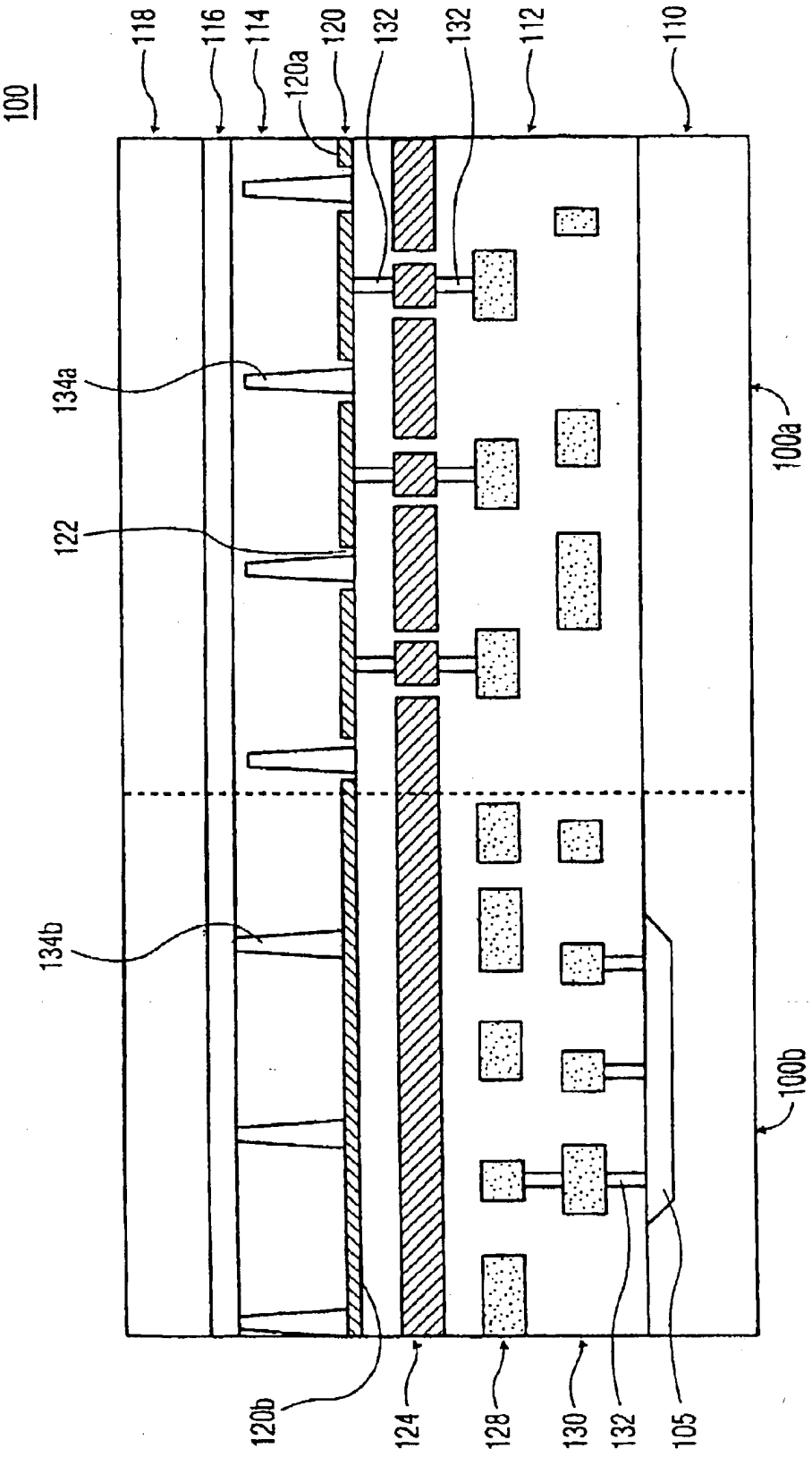
Primary Examiner—Toan Ton

(57) **ABSTRACT**

A reflective liquid crystal display (LCD) device includes a plurality of openings patterned in the pixel metal layer in the peripheral region of the device exposing the insulating layer beneath, a plurality of light-shielding islands beneath the openings in the pixel metal layer, and a plurality of walls formed on the islands surrounding the openings and extending substantially between the islands and the pixel metal layer. A plurality of spacers are disposed on the exposed portions of the insulating layer in the peripheral region for supporting the transparent (e.g., glass) layer above and providing a space for the liquid crystal material. The structure enhances display uniformity by making the spacers formed in the peripheral area more closely match the spacers formed in the pixel area of the device. The structure also prevents light from reaching the substrate in the peripheral region of the device and permits portions of the second metal layer formed in the peripheral region of the device to be used for signal routing.

4 Claims, 3 Drawing Sheets




100
118
116
114
120a
120
132
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112
110
134a
122
134b
100a
100b
120b
124
128
130
132
105

FIG. 1

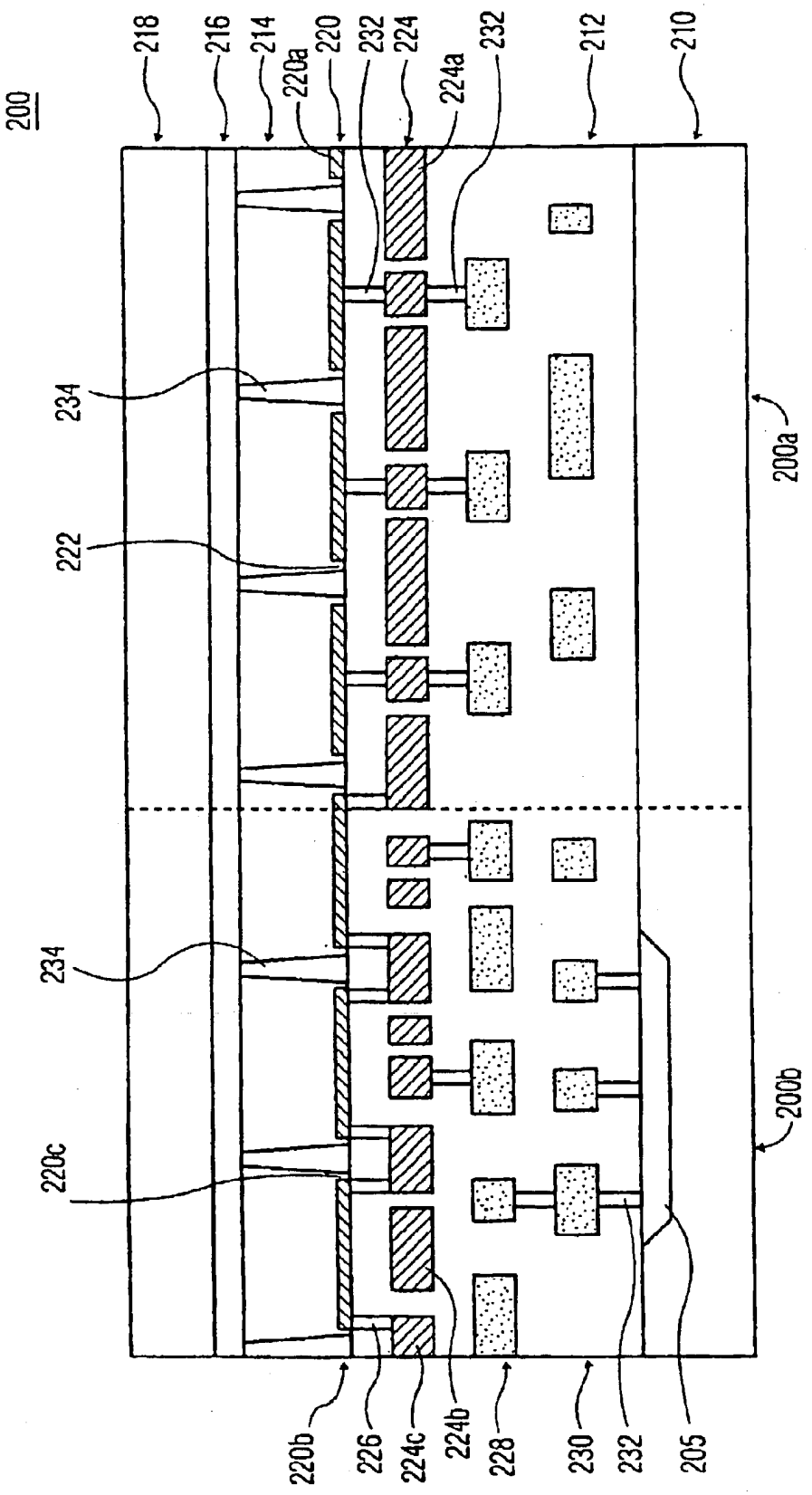
200
218
216
214
220a
220
232
224
224a
232
212
210
234
222
234
220c
200a
200b
220b
226
224c
224b
228
230
232
205

FIG. 2

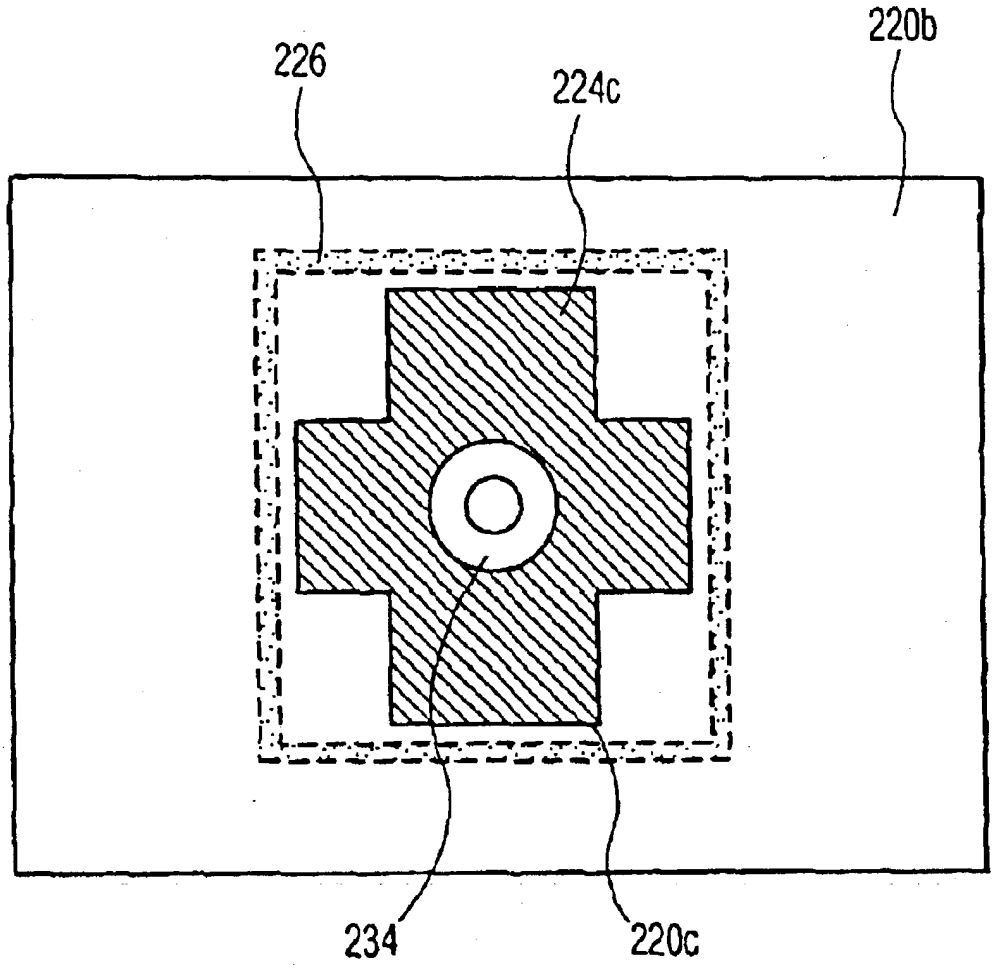

FIG. 3

LIQUID CRYSTAL DISPLAY DEVICE HAVING UNIFORM INTEGRATED SPACERS

This is a divisional of application Ser. No. 09/833,718, filed Apr. 13, 2001, now U.S. Pat. No. 6,642,986.

BACKGROUND OF THE INVENTION

1) Field of the Invention

This invention pertains to the field of liquid crystal display (LCD) devices, such as liquid crystal on silicon (LCOS) devices, and more particularly to a structure for such a device providing for uniform spacers.

2) Description of the Related Art

Reflective LCD devices are well known. Examples of such devices, and in particular active matrix devices, are shown in U.S. Pat. Nos. 6,023,309 and 6,052,165. With reference to the following description, familiarity with conventional features of such devices will be assumed, so that only features bearing on the present invention will be described.

FIG. **1** shows a portion of a typical prior-art reflective LCD device **100**. The reflective LCD device **100** may generally be divided into a pixel region **100***a* (active region) and a peripheral region **100***b*. The pixel region **100***a* includes an array of pixel elements and the peripheral region **100***b* includes driver circuits **105** for supplying driving signals to each of the pixel elements.

The LCD device **100** comprises, in relevant part, a silicon substrate **110**, an insulating layer **112**, a liquid crystal layer **114** a transparent electrode **116**, such as indium-tin-oxide (ITO), and a transparent (e.g., glass) layer **118**. A reflective mirror (pixel) metal layer **120** is provided beneath the liquid crystal layer **114** on the insulating layer **112**. The mirror metal layer **120** includes a plurality of individual reflective pixel electrodes **120***a* in the pixel region **100***a*, and a substantially continuous peripheral portion **120***b* formed in the peripheral region **100***b* of the LCD device **200**. Light transmissive regions **122** are located between the pixel electrodes **120***a*.

Also provided in the insulating layer **112** and between the mirror metal layer **120** and the substrate **110** are a light shield metal layer **124** and routing metal layers, **128** and **130**. In the pixel region **100***a*, the metal layers **128** and **130** form mutually-orthogonal row and column lines, which may be connected to gate and source electrodes of MOS transistors (not shown in FIG. **1**) for pixel elements fabricated in the underlying substrate **110**. In the peripheral region **100***b*, the metal layers **128** and **130** form signal routing lines used for routing various signals of the driver circuits. Also, metal plugs or vias **132** are provided for connecting various portions of the light shield metal layer **124** and the third and fourth metal layers **128**, **130** with each other.

The metal layer **124** is provided to prevent light entering the device, such as through the transmissive regions **122** between the pixel electrodes **120***a*, from reaching the substrate **110** where it might induce leakage currents on otherwise interfere with proper device operation. While portions of metal layers **128** or **130** may incidentally block a small portion of light entering the device, the structure of FIG. **1** requires a separate metal layer **124** to be dedicated to provide the required degree of light blocking in the peripheral region **100***b*.

A plurality of spacers or pillars are provided for supporting the transparent layer **118** and providing a gap for the liquid crystal layer **114**. In the pixel region **100***a*, the spacers **134***a* are placed directly on the insulating layer **112**. In the peripheral region **100***b*, spacers **134***b* are provided on the peripheral portion **120***b* of the mirror metal layer **120**.

In order to maintain a uniform liquid crystal cell gap, it becomes necessary for the spacers in the peripheral region **100***b* to have a height that is the same as the spacers in the pixel region **100***a*. However, the spacers **134***b* formed on the mirror metal layer **120** in the peripheral region **100***b* are taller than the spacers **134***a* formed on the insulating layer **112** in the pixel region **100***a* because of the extra height of the metal layer **120**, thus producing a non-uniform display.

Accordingly, it would be desirable to provide a liquid crystal display device having spacers with a more uniform height in both the pixel and peripheral regions of a reflective LCD device. Other and further objects and advantages will appear hereinafter.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a liquid crystal display (LCD) device having a more uniform spacer structure.

In accordance with one aspect of the invention, an LCD device is provided having a pixel region and a peripheral region adjacent to the pixel region, comprising a silicon substrate, an insulating layer on the substrate, a first metal layer above the insulating layer including an array of pixel electrodes in the pixel region and a peripheral portion in the peripheral region having a plurality of openings therein, a plurality of spacers in the openings, a second metal layer between the first metal layer and the substrate, and a plurality of walls each corresponding to one of the plurality of openings and extending substantially between the second metal layer and the first metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a simplified cross-sectional view of a portion of a prior-art liquid crystal display (LCD) device;

FIG. **2** shows a simplified cross-sectional view of a portion of one embodiment of an LCD device having integrated spacers in accordance with one or more aspects of the invention; and

FIG. **3** shows a top plan view of a portion of the LCD device shown in FIG. **2**.

DETAILED DESCRIPTION

FIG. **2** shows a simplified cross-sectional view of a portion of a reflective LCD device **200** in accordance with one or more aspects of the invention. For clarity, those portions of the device relating to the present invention are illustrated. The reflective LCD device **200** may generally be divided into a pixel region **200***a* (active region) and a peripheral region **200***b*. The pixel region **200***a* includes an array of pixel elements, and the peripheral region **200***b* includes driver circuits (not shown in FIG. **2**) for supplying driving signals to each of the pixel elements.

The LCD device **200** comprises, in relevant part, a silicon substrate **210** on which are successively provided an insulating layer **212**, a liquid crystal layer **214**, a transparent electrode **216**, such as indium-tin-oxide (ITO), and a transparent (e.g., glass) layer **218**. A first metal layer **220** is provided on the insulating layer **212** beneath the liquid crystal layer **214**. The first metal layer **220** includes a plurality of individual reflective pixel electrodes **220***a* formed in the pixel region **200***a*, and a peripheral portion **220***b* formed in the peripheral region **200***b* of the LCD

device **200**. Light transmissive regions **222** are located between the pixel electrodes **220***a*. A plurality of openings **220***c* are formed in the peripheral portion **220***b* of the first metal layer **220**, each opening exposing a portion of the insulating layer **212**.

Also, a second metal layer **224** is provided between the first metal layer **220** and the substrate **210**. The second metal layer **224** includes a light shield portion **224***a* in the pixel region **200***a*, and a plurality of signal routing lines **224***b* and light shields **224***c* in the peripheral region **200***b*. At each of the light shields **224***c* is provided a light-blocking partition or wall **226** extending substantially between the light shield **224***c* and the peripheral portion **220***b* of the first metal layer **220**. Third and fourth metal layers **228** and **230** are provided between the second metal layer **224** and the substrate **210**. Also, metal plugs or vias **232** are provided for connecting various portions of the second, third, and fourth metal layers with each other.

A plurality of integrated spacers or pillars **234** are provided for supporting the transparent electrode **216** and transparent layer **218** and providing a gap for the liquid crystal layer **214**. In the pixel region **200***a*, the spacers **234** are placed directly on the insulating layer **212** in the light transmissive regions **222** between the pixel electrodes **220***a*. In the peripheral region, the spacers **234** are located on the openings **220***c* in the peripheral portion **220***b* of the first metal layer **220**. Preferably, the spacers **234** may be formed by uniformly applying a coating (e.g., Si_3N_4; SiO_2) over the first metal layer **220** and exposed insulating layer **212** to a desired height, and etching the coated material to produce the spacers **234**. The height and diameter of the spacers **234** are selected to provide the desired gap for the liquid crystal layer **214**, and the required strength to support the transparent layer **218**. In one embodiment, the spacers **234** may have a height of 1–2 μm, and as small a diameter as 0.4 μm. Larger spacers, which simply the manufacturing process, may also be employed.

An operation of various pertinent elements of the embodiment will now be described.

Beneficially, the first metal layer **220** is a mirror (pixel) metal layer, such that it blocks light which directly impinges on it from reaching the substrate **210**. However, openings **220***c* are produced in the peripheral portion **220***b* of the first metal layer **220** in the peripheral region **200***b* so that the spacers **234** in the peripheral region **200***b* may be of a uniform height with the spacers **234** in the pixel region **200***a*. Accordingly, it is necessary to prevent light which impinges on the openings **220***c* from reaching the substrate **210**.

For this purpose, it is possible to use the second metal layer **224** as a substantially continuous dedicated light shielding area covering the entire peripheral region **220***b*. In that case, any light which would pass through the openings **220***c* in the first metal layer **220** would be blocked by the second metal layer **224** from reaching the substrate **210** in the peripheral region **200***b*.

However, the area required for the driver circuits **205** can be reduced if the metal layer **224** could also be used for routing driver circuitry signals in the peripheral region **200***b*, instead of being dedicated only to light blocking.

Accordingly, in the preferred embodiment, the second metal layer **224** includes the light shields **224***c* in the peripheral region **200***b* arranged beneath each of the openings **220***c*. Preferably, each light shield **224***c* is an island, substantially disconnected from a remainder of the second metal layer **224**. Additionally, on each of the light shields **224***c* is provided the light-blocking partition or wall **226** extending substantially between the light shield **224***c* and the peripheral portion **220***b* of the first metal layer **220**. Preferably, the wall **226** is continuously formed around the entire opening **220***c*. Also, preferably, the wall **226** extends vertically to connect the light shield **224***c* to the peripheral portion **220***b* of the first metal layer **220**.

FIG. **3** shows a top plan view of a portion of the peripheral region **200***b* of the LCD device **200** in the vicinity of one of the openings **220***c* in the first metal layer **220**. As shown in FIG. **3**, in one embodiment the opening **220***c* in the peripheral portion **220***b* of the first metal layer **220** is in the shape of a cross, and the spacer **234** is located in the middle of the intersection of the cross. In one embodiment, the end-to-end length of the "cross" in each of the "x" and "y" directions is 1.2 μm. This mimics the area between pixel electrodes **220***a* where the spacers **234** are located in the pixel region **200***a*, producing better display uniformity.

Meanwhile, the light shield **224***c* is an island that may be of any convenient size or shape, so long as it is at least as large as the opening **220***c*. In one embodiment, the length of the light shield in each of the "x" and "y" directions is 3.5 μm. The wall **226** may also be of any convenient size or shape, so long as it substantially encloses the opening **220***c*, and is no larger than the light shield **224***c*.

Preferably, the wall **226** is formed by patterning a vertically-extending via in the insulating layer **212** and depositing a light-blocking material therein prior to depositing the first metal layer **220**. The wall **226** may be formed in a same step as the formation of the metal plugs **232** connected to the pixel electrodes **220***a*. Also, preferably, the wall **226** is formed of Tungsten. In this case, the wall **226** is formed of the same material as the vias **232** in the insulating layer **212**, thus requiring no additional processing steps. However, other light blocking materials and methods of fabrication may be used. In one embodiment, the wall **226** has a height of approximately 1 μm so as to extend vertically between and connect the first metal layer **220** and the second metal layer **224**. In that case, the thickness of the wall **226** may be approximately 0.4 μm.

While the present invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in detail may be made without departing from the scope of the invention as defined by the claims.

What is claimed is:

1. A method of producing a liquid crystal display (LCD) device having a pixel region and a peripheral region adjacent to the pixel region, comprising:

forming an insulating layer on a substrate;

forming a first metal layer above the substrate;

forming a pixel metal layer above the first metal layer, the pixel metal layer comprising an array of pixel electrodes in the pixel region, and a peripheral portion in the peripheral region having a plurality of openings therein exposing portions of the insulating layer; and

forming a plurality of walls, each corresponding to a corresponding one of the plurality of openings and extending substantially between the first metal layer and the peripheral portion of the pixel metal layer.

2. The method of claim **1**, wherein forming the first metal layer comprises:

forming a plurality of light shields directly beneath the openings in the peripheral portion of the pixel metal layer, and

forming a plurality of signal routing lines in the peripheral region.

3. The method of claim **1**, wherein each wall is formed substantially continuously around the corresponding opening.

4. The method of claim **1**, wherein the wall is formed of an opaque material.

* * * * *